

WE CLAIM:

1. A test signal attenuation circuit comprising:
a signal transmitter;
a circuit for generating a binary-level waveform;
a circuit for providing a chopping signal for a square type
5 waveform; and
a circuit for combining said binary-level waveform and said chopping signal to produce an attenuated chopped signal having less energy content than said original, generated binary-level waveform.
- 2.. The attenuation circuit of claim 1 wherein said chopping circuit provides an attenuated chopped signal having a narrower pulse width than the original binary-level waveform.
3. The attenuation circuit of claim 2 wherein said chopping circuit provides an attenuated chopped signal having the same amplitude as the original binary-level waveform.
4. The attenuation circuit of claim 3 further including a pulse shaping circuit for forming attenuated pulses in the chopped attenuated signal.
5. The attenuation circuit of claim 4 wherein said pulse shaping circuit converts clock pulses into the attenuated chopped signal waveform.
6. The attenuated circuit of claim 4 including a pulse shaping circuit for forming attenuated pulses in the chopped attenuated signal.
- 7.. The attenuated circuit of claim 6 wherein said pulse shaping circuit converts clock pulses into the attenuated chopped signal waveform.

- 8.. A test signal attenuation circuit comprising:
a signal transmitter;
a circuit for generating a binary-level waveform;
a circuit for providing a chopping signal for a binary-level
5 waveform; and
a chopping circuit for combining said binary-level waveform and
said chopping signal to produce an attenuated chopped signal having less
energy content than said original binary-level waveform;
said chopping circuit providing an attenuated chopped signal
10 having a narrower pulse width than the original binary-level waveform.
- 9.. The test signal attenuation circuit of claim 8 wherein said chopping
circuit provides an attenuated chopped signal having the same amplitude as the
original binary-level waveform.
10. The test signal attenuation circuit of claim 9 further including a
pulse shaping circuit for forming attenuated pulses in the chopped attenuated
signal.
11. The test signal attenuation circuit of claim 10 wherein said pulse
shaping circuit converts clock pulses into the attenuated chopped signal
waveform.

12. A test signal attenuation circuit comprising:
a signal transmitter;
a circuit for generating a binary-level waveform;
a circuit for providing a chopping signal for a binary-level
5 waveform;

a chopping circuit for combining said binary-level waveform and
said chopping signal to produce an attenuated chopped signal having less
energy content than said original, generated binary-level waveform; and
said chopping circuit providing an attenuated chopped signal
10 having a narrower pulse width than the original binary-level waveform.

13. The test signal attenuation circuit of claim 12 wherein said
chopping circuit provides an attenuated chopping signal having the same
amplitude as the original binary-level waveform.

14. A method of developing an electrical test signal comprising the
steps of:

activating a signal transmitter;
generating a binary-level waveform;
5 providing a chopping signal for a square type waveform; and
combining said binary-level waveform and said chopping
signal to produce an attenuated chopped signal having less energy content than
the original binary-level waveform.